PASS GATE MULTIPLEXER CIRCUIT WITH REDUCED SUSCEPTIBILITY TO SINGLE EVENT UPSETS

ABSTRACT

A multiplexer circuit for programmable logic devices (PLDs) has reduced susceptibility to single event upsets. The pass gate multiplexer circuit has N pass gates and N memory cells controlling the pass gates. Each path between an input terminal and the output node includes two pass gates controlled by different memory cells. Therefore, a single event upset that inadvertently enables a pass gate can only short two input terminals when the other pass gate in the affected input path is also enabled by its associated memory cell. Therefore, the multiplexer circuit with two pass gates in each input path reduces the susceptibility to single event upsets by a factor of (N-4)/N.